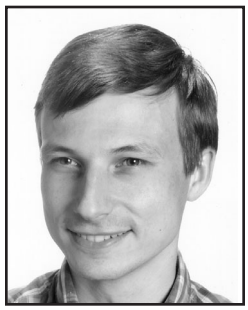
Session 3 Overview

Oversampling ADCs



Chair: Raf Roovers, Philips, Eindhoven, The Netherlands

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The increasing data rates in both wired and wireless communication systems constantly demands higher SNR and bandwidth requirements in the receiver and the ADC. Moreover, a clear trend to digitize receivers as much as possible by pushing the ADC towards the antenna, results in even more challenging ADC requirements. During recent years, oversampling ADCs have continuously increased their conversion bandwidth and dynamic range and are becoming a feasible ADC approach for many of the existing and new communication standards. Due to their power efficiency, oversampling ADCs are very suitable for efficient receiver implementation.

In paper 3.1 a power-efficient ΔΣ ADC with a SNDR of 74dB in a signal bandwidth of 20MHz is realized in a 0.13μm standard CMOS technology. The power consumption of only 20mW is achieved with a multi-bit single loop topology using a direct quantizer feedback technique. A PLL is integrated with the ΔΣ ADC to generate the required low jitter clock.

The next two papers demonstrate converters that directly handle IF receiver signals. Paper 3.2 presents a quadrature bandpass ΔΣ ADC that achieves 90dB dynamic range for a universal TV receiver with a bandwidth of 8.5MHz around 44MHz. Paper 3.3 describes a topology, where a mixer is integrated in front of the ΔΣ ADC to achieve 118dB dynamic range for AM and FM radio application in a bandwidth of 3kHz around 10.7MHz.

Paper 3.4 and 5 demonstrate the power efficiency of oversampling ADCs for wireline communication applications such as ADSL. Paper 3.4 introduces a combined analog and digital feedforward topology to achieve an 86dB DR in a 2.2MHz signal bandwidth for only 14mW. Paper 3.5 implements a time-interleaved topology resulting in a DR of 85dB over a 1.1MHz signal bandwidth with only 5.4mW. Both converters are realized in a 0.18μm CMOS technology.

Two papers in this session demonstrate that ΔΣ ADCs can operate from a sub 1V supply. Paper 3.6 describes a ΔΣ ADC operating at a supply voltage as low as 0.5V in a 0.18μm triple-well CMOS technology. Despite this low voltage, a peak SNDR of 74dB is obtained in a 25kHz bandwidth by using body-input circuits. Paper 3.7 presents a 0.9V ΔΣ modulator using a single-phase sampling technique and opamp sharing to achieve an SNDR of 80dB in 10kHz bandwidth with 0.2mW.

Finally, Paper 3.8 demonstrates a multi-bit switched-capacitor ΔΣ ADC in 0.18μm CMOS for digital TV receivers. A new double-sampling scheme is applied that enables the ADC to achieve an SNDR of 76.3dB over a 3.2MHz bandwidth.

3.1 A 14b 20mW 640MHz CMOS CT ΔΣ ADC with 20MHz Signal Bandwidth and 12b ENOB **1:30 PM**

G. Mitteregger, Xignal Technologies, Unterhaching, Germany

A 3rd-order single-loop CT ΔΣ modulator with a 4b internal quantizer operating at 640MHz achieves 76dB SNR, -78dB THD, and 74dB SINAD in a 20MHz signal bandwidth with an OSR of 16. The modulator operates between 20 to 40MS/s output data rate and dissipates 20mW from a 1.2V supply at 40MS/s. The degradation of stability due to excess loop delay is solved with a quantizer feedback architecture.

3.2 A 375mW Quadrature Bandpass ΔΣ ADC with 90dB DR and 8.5MHz BW at 44MHz **2:00 PM**

R. Schreier, Analog Devices, Wilmington, MA

A CT quadrature bandpass ADC is designed for a multi-standard television receiver. When clocked at 264MHz, the ADC achieves 90dB of total DR over an 8.5MHz BW centered at 44MHz. The 4th-order 4b ADC uses a modified feedforward topology and includes 12dB of AGC. The 2.5mm^2 chip consumes 375mW in a 0.18µm CMOS process.

3.3 A 118dB DR CT IF-to-Baseband ΣΔ Modulator for AM/FM/IBOC Radio Receivers **2:30 PM**

P. Silva, Delft University of Technology, Delft, The Netherlands

A 1b 5th-order complex CT ΣΔ modulator with integrated IF mixer for AM/FM/IBOC car radio receivers is presented. The 118dB DR in AM mode enables the realization of the receiver without a VGA and an external AM channel filter. It is fabricated in a 0.18µm CMOS process and consumes 210mW from a 1.8V supply.

3.4 A 14mW Multi-bit ΔΣ Modulator with 82dB SNR and 86dB DR for ADSL2+ **3:15 PM**

S. Kwon, University of Texas at Dallas, Richardson, TX

Analog and digital feedforward swing-reduction techniques optimize the power consumption of this 2nd-order ΔΣ modulator. The 0.18µm CMOS prototype uses 2 telescopic OTAs and 2 ADCs requiring 10 comparators. The technique makes the modulator equivalent to a 4b architecture. The OSR is 33 and the clock frequency is 144MHz.

3.5 A 5.4mW 2-Channel Time-Interleaved Multi-bit ΔΣ Modulator with 80dB SNR and 85dB DR for ADSL **3:45 PM**

K-S. Lee, University of Texas at Dallas, Richardson, TX

A 2nd-order ΔΣ modulator that obtains low power consumption by 2-channel time-interleaving is described. The main channel requires 2 opamps whereas the second channel does not use any active elements. This structure is robust to channel mismatches and uses a simple clocking scheme. The circuit is integrated in a 0.18µm CMOS process and occupies an active area of 1.1mm^2.

3.6 A 0.5V 74dB SNDR 25kHz CT ΔΣ Modulator with Return-to-Open DAC **4:15 PM**

K-P. Pun, Chinese University of Hong Kong, Hong Kong, China

A 0.5V 3rd-order 1b fully differential CT ΔΣ modulator in a 0.18µm CMOS process is presented. A special return-to-open DAC, a body-input gate-clocked comparator, and body-input OTAs for the active-RC loop filter enable the ultra-low voltage operation. The 0.6mm^2 chip consumes 370µW and achieves a peak SNDR of 74dB in a 25kHz BW.

3.7 A 0.9V ΔΣ Modulator with 80dB SNDR and 83dB DR Using a Single-Phase Technique **4:45 PM**

N. Paulino, Universidade Nova de Lisboa, Monte da Caparica, Portugal

A 2nd-order ΔΣ ADC implemented in 0.18µm CMOS occupies 0.06mm^2 and dissipates 0.2mW from a 0.9V supply. It achieves 80dB SNDR and 83dB DR over a 10kHz BW employing a single-phase technique to reach such performance. An amplifier-sharing scheme is proposed to improve power and area efficiency.

3.8 A 80/100MS/s 76.3/70.1dB SNDR ΔΣ ADC for Digital TV Receivers **5:00 PM**

Y. Fujimoto, SHARP, Nara, Japan

A 4th-order SC ΔΣ modulator with a 4b quantizer is designed for a low-power direct-conversion receiver SoC for Japanese ISDB-T and European DVB-T. It achieves a 76.3/70.1dB SNDR over a 3.2/4MHz bandwidth with a clock frequency of 80/100MHz. The 1.7mm^2 chip, fabricated in a 0.18µm CMOS process draws 13.2/19.1mA from a 1.8V supply. It has a FOM of 0.7/1.64pJ/conversion.